ANALOG ELECTRONIC CIRCUITS
LAB MANUAL

III SEMESTER B.E (E & C)
(For private circulation only)

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Design :-

Given: $V_{cc} = 15 \text{ V}; \quad I_e = 1 \text{ mA}; \quad A_v = 50; \quad f_l = 500 \text{ Hz}; \quad$ Stability factor $= [2-10]$.

Gain formula is given by,

$$A_v = \frac{-h_{fe} R_{I,eff}}{h_{ie}}$$

Assume, $V_{CE} = \frac{V_{CC}}{2}$ (Active condition); $V_E = \frac{V_{CC}}{10}$

Effective load resistance is given by $R_{I,eff} = R_C \parallel R_L$.

Internal emitter resistance is given by $r_e = \frac{26 \text{ mV}}{I_E}$

$$h_{ie} = \beta r_e$$

where $r_e$ is internal emitter resistance of the transistor.

$$h_{ie} = h_{fe} r_e$$

On applying KVL to output loop, we get

$$V_{cc} = I_C R_C + V_{CE} + I_E R_E$$

where

$$V_E = I_E R_E$$

$$R_C = ?$$
AIM: -To design a RC coupled single stage FET/BJT amplifier and determination of the gain-frequency response, input and output impedances.

APPARATUS REQUIRED:-

Transistor - BC 107, capacitors, resistor, power supply, CRO, function generator, multimeter, etc.

PROCEDURE: -

1. Connect the circuit as per the circuit diagram.
2. Set $V_s = 50mV$ (assume) using the signal generator
3. Keeping the input voltage constant, vary the frequency from 0Hz to 1MHz in regular steps of 10 and note down corresponding output voltage.
4. Plot the frequency response: Gain (dB) vs Frequency (Hz).
5. Find the input and output impedance.
6. Calculate the bandwidth from the graph.
7. Note down the phase angle, bandwidth, input and output impedance.
The emitter current is given by the equation \( I_E = I_B + I_C \).
Since \( I_B \) is very small when compared with \( I_C \),

\[
I_C \approx I_E
\]

\[
R_E = \frac{V_E}{I_E} = ?
\]

The voltage at the base of the transistor is given by

\[
V_B = V_{BE} + V_E
\]

From voltage divider rule, the voltage at the base of the transistor is given by

\[
V_B = V_{CC} \cdot \frac{R_{B2}}{R_{B1} + R_{B2}}
\]

The equation for stability factor is given by

\[
S = 1 + \frac{R_B}{R_E}
\]

Find \( R_B \)

\[
R_B = R_{B1} \parallel R_{B2}
\]

From equations (i) and (ii), solve for \( R_{B1} \) and \( R_{B2} \)

Input coupling capacitor is given by,

\[
X_{CI} = \frac{\left( h_{ie} \parallel R_B \right)}{10}
\]

\[
X_{C1} = \frac{1}{2\pi f C_i}
\]

\[
C_i = ?
\]

Output coupling capacitor is given by

\[
X_{C0} = \frac{R_C \parallel R_I}{10}
\]

\[
X_{C0} = \frac{1}{2\pi f C_0}
\]

\[
C_0 = ?
\]

By-pass capacitor is given by, \( X_{CE} = \frac{R'_E}{10} \)

where,

\[
R'_E = \left[ R_E \parallel \frac{(R_B + h_{ie})}{h_{fe}} \right]
\]

\[
X_{CE} = \frac{1}{2\pi f C_E}
\]

\[
C_E = ?
\]
**General Procedure for Calculation :-**

1. **Input impedance**
   a. Connect a Decade Resistance Box (DRB) between input voltage source and the base of the transistor (series connection).
   b. Connect ac voltmeter (0-100mV) across the biasing resistor $R_2$.
   c. Vary the value of DRB such that the ac voltmeter reads the voltage half of the input signal.
   d. Note down the resistance of the DRB, which is the input impedance.

2. **Output impedance**
   a. Measure the output voltage when the amplifier is operating in the mid-band frequency with load resistance connected ($V_{\text{load}}$).
   b. Measure the output voltage when the amplifier is operating in the mid-band frequency without load resistance connected ($V_{\text{no-load}}$).
   c. Substitute these values in the formula $Z_O = \frac{V_{\text{load}} - V_{\text{no-load}}}{V_{\text{load}}} \times 100\%$

3. **Bandwidth**
   a. Plot the frequency response
   b. Identify the maximum gain region.
   c. Drop a horizontal line bi –3dB.
   d. The –3dB line intersects the frequency response plot at two points.
   e. The lower intersecting point of –3dB line with the frequency response plot gives the lower cut-off frequency.
   f. The upper intersecting point of –3dB line with the frequency response plot gives the upper cut-off frequency.
   g. The difference between upper cut-off frequency and lower cut-off frequency is called Bandwidth. Thus Bandwidth = $f_h - f_l$. 
Model Graph (Frequency Response) :-

![Model Graph](image)

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</table>
Circuit Diagram :-

DC Analysis :-
Experiment No: DATE: __/__/____

**DARLINGTON EMITTER FOLLOWER**

To design a BJT Darlington Emitter follower and determine the gain, input and output impedances.

**AIM:**

**APPARATUS REQUIRED:**

Transistor - BC 107, capacitors, resistor, power supply, CRO, function generator, multimeter, etc.

**PROCEDURE:**

1. Connect the circuit as per the circuit diagram.
2. Set $V_i = 1$ volt (say), using the signal generator.
3. Keeping the input voltage constant, vary the frequency from 0Hz to 1MHz in regular steps of 10 and note down corresponding output voltage.
4. Plot the frequency response: Gain (dB) vs Frequency (Hz).
5. Find the input and output impedance.
6. Calculate the bandwidth from the graph.
7. Note down the phase angle, bandwidth, input and output impedance.
Design :-

Given \( V_{CEQ} = V_{CE2} = 6v \)
\( I_{CQ} = I_{C2} = 5mA \)

Assume \( \beta \) for SL100 = 100
\( V_{CC} = 12v \)

\[
V_{E2} = \frac{V_{CC}}{2} = \frac{12}{2} = 6v
\]

\[
I_{E2}R_E = V_{E2}
\]

\[
\therefore R_E = \frac{V_{E2}}{I_{E2}} = \frac{6}{5 \times 10^{-3}} = 1.2k\Omega \quad [\therefore I_E = I_C]
\]

\[
\therefore R_E = 1.2k\Omega
\]

\( V_B1 = VBE_1 + VBE_2 + VE_2 \)

\( V_B1 = 0.7 + 0.7 + 6 \)

\( V_B1 = 7.4v \)

\[
I_{B2} = \frac{I_{C2}}{\beta} = \frac{5 \times 10^{-3}}{100} = 0.05mA
\]

\[
I_{B1} = \frac{I_{C1}}{\beta} = \frac{I_{B2}}{\beta} = \frac{0.05}{100} = 0.0005mA
\]

\[
10I_B1R_1 = V_{CC} - V_B1
\]

\[
\therefore R_1 = \frac{12 - 7.4}{10 \times 0.0005 \times 10^{-3}} = 920k\Omega \quad [\text{Use } R_1 = 1M\Omega]
\]

\[
R_2 = \frac{V_{B1}}{9I_B} = 1644k\Omega
\]

\[
\therefore R_2 = 1.5M\Omega
\]
**General Procedure for Calculation:**

1. **Input impedance**
   
   a. Connect a Decade Resistance Box (DRB) between input voltage source and the base of the transistor (series connection).
   
   b. Connect ac voltmeter (0-100mV) across the biasing resistor $R_2$.
   
   c. Vary the value of DRB such that the ac voltmeter reads the voltage half of the input signal.
   
   d. Note down the resistance of the DRB, which is the input impedance.

2. **Output impedance**
   
   a. Measure the output voltage when the amplifier is operating in the mid-band frequency with load resistance connected ($V_{\text{load}}$).
   
   b. Measure the output voltage when the amplifier is operating in the mid-band frequency without load resistance connected ($V_{\text{no-load}}$).
   
   c. Substitute these values in the formula $Z_o = \frac{V_{\text{load}} - V_{\text{no-load}}}{V_{\text{load}}} \times 100\%$

3. **Bandwidth**
   
   a. Plot the frequency response.
   
   b. Identify the maximum gain region.
   
   c. Drop a horizontal line bi –3dB.
   
   d. The –3dB line intersects the frequency response plot at two points.
   
   e. The lower intersecting point of –3dB line with the frequency response plot gives the lower cut-off frequency.
   
   f. The upper intersecting point of –3dB line with the frequency response plot gives the upper cut-off frequency.
   
   g. The difference between upper cut-off frequency and lower cut-off frequency is called Bandwidth. Thus Bandwidth = $f_h - f_l$. 

Model Graph: (Frequency Response)

![Model Graph]

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</table>
4. To find Q-Point

a. Connect the circuit as per circuit diagram

b. Switch on the DC source [switch off the AC source]

c. Measure voltage at \( V_{B2} \), \( V_{E2} \) & \( V_{C2} \) with respect to ground \\
   & also measure \( V_{CE2} = V_{C2} - V_{E2} \) \\
   \( I_{C2} = \frac{V_{E2}}{R_E} \) \\
   Q-Point = \([V_{CE2}, I_{C2}]\)

Result

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Circuit Diagram :-

Amplifier without Feedback

Amplifier with Feedback

$V_i = 50\text{mV}$
Freq. = (0–1) MHz
Experiment No: ___________________ DATE: __/__/____

VOLTAGE SERIES FEEDBACK AMPLIFIER

To design a FET/BJT Voltage series feedback amplifier and determine the gain, frequency response, input and output impedances with and without feedback

AIM: -

APPARATUS REQUIRED:-

Transistor - BC 107, capacitors, resistor, power supply, CRO, function generator, multimeter, etc.

PROCEDURE: -

1. Connect the circuit as per the circuit diagram.
2. Set Vs = 50mV (assume) using the signal generator
3. Keeping the input voltage constant, vary the frequency from 0Hz to 1MHz in regular steps of 10 and note down corresponding output voltage.
4. Plot the frequency response: Gain (dB) vs Frequency (Hz).
5. Find the input and output impedance.
6. Calculate the bandwidth from the graph.
7. Note down the phase angle, bandwidth, input and output impedance.
**Design (With Feedback):**

Given $A_{V1} = 30; A_{12} = 20; V_{CC} = 10V; I_{E2} = 1.8mA; I_{E1} = 1.1mA; S = 3; h_{fe1}$ and $h_{fe2}$ are obtained by multimeter $\beta = 0.03$

**DC Analysis of II Stage:**

$$V_{CC} = I_{C2}R_{C2} + V_{CE2} + I_{E2}R_{E2}$$

$R_{B1} = (S-1) R_{E1} = ?$

$R_{B1} = R_1 \parallel R_2$

find $R_1$ and $R_2$

Input impedance is given by

$$Z_{ii} = R_{B1} \parallel [h_{fe1} + (1 + h_{fe1}) R_{f1}]$$

Output impedance is given by

$$Z_{o1} = R_{C1}$$

The feedback factor $\beta$ is given by

$$\beta = \frac{R_{f1}}{R_{f1} + R_{f2}}$$

where, $R_{f2} >> R_{f1}$

assume $R_{f2} = 10 k\Omega$; find $R_{f1}$

overall voltage gain is given by

$$A_V = A_{V1} \times A_{V2}$$

**Parameter Analysis with Feedback**

The desensitive factor, $D = 1 + \beta A_V$

Output impedance with feedback is given by

$$Z_{of} = \frac{Z_{o2}}{D}$$

Input impedance with feedback is given by

$$Z_{if} = Z_{ii} \times D$$

The gain with feedback is given by

$$A_{if} = \frac{A_V}{D}$$

The output capacitor is given by

$$X_{C0} = \frac{Z_{o2}}{10}$$

where $X_{C0} = \frac{1}{2\pi fC_0}$

$C_0 = ?$
The input capacitor is given by,

\[ X_{Ci} = \frac{Z_{in}}{10} \]

where \( X_{Ci} = \frac{1}{2\pi f_{Ci}} \)

\( C_i = ? \)

for active condition, \( V_{CE2} = \frac{V_{CC}}{2} \)

The voltage gain is given by

\[ A_{V2} = \frac{-h_{fe2} R_C2}{h_{ie2}} \]

\( R_{C2} = ? \)

\[ R_{E2} = \frac{V_{CC} - V_{CE2} - I_{C2} R_{C2}}{I_{E2}} = ? \]

\[ V_{B2} - V_{BE} + V_{E2} - \frac{V_{CC}}{R_3 + R_4} \times R_4 \]

\[ S = 1 + \frac{R_{B2}}{R_{E2}} \]

\( R_{B2} = (S-1) R_{E2} = ? \)

\( R_{B2} = R_3 \parallel R_4 \)

on solving (i) and (ii)

Find \( R_3 \) and \( R_4 \).

Input impedance is given by,

\[ Z_{i2} = (R_{B2} \parallel h_{ie2}) \]

Output impedance is given by,

\[ Z_{o2} = R_{C2} \]

**DC Analysis of I Stage**

The voltage gain is given by

\[ A_{V1} = \frac{-h_{fe1}(R_{C1} \parallel Z_{iC})}{h_{ie1}} \]

\((R_{C1} \parallel Z_{i2}) = ? \)

Find \( R_{C1} = ? \)
Apply KVL to first stage,

\[ V_{CC} = I_{C1} R_{C1} + V_{CE1} + I_{E1} R_{E1} \]

for active condition, \( V_{CE1} = \frac{V_{CC}}{2} \)

\[ V_{E1} = \frac{V_{CC} - V_{CE1} - I_{C1} R_{C1}}{I_{E1}} \]

\[ V_{B1} = V_{BE} + V_{E1} = \frac{V_{CC}}{R_1 + R_2} \times R_2 \]

\[ S = 1 + \frac{R_{B1}}{R_{E1}} \]

The emitter capacitor of first stage is given by

\[ X_{CE} = \frac{R'_{E1}}{10} \quad \text{where} \quad R'_{E1} = R_E || \left( R_f 1 + \frac{R_{B1} + h_{fe2}}{1 + h_{fe2}} \right) \]

The emitter capacitor of II stage is given by

\[ X_{CE2} = \frac{R'_{E2}}{10} \quad \text{where} \quad R'_{E2} = R_{E2} || \left( \frac{h_{fe2} + R_{B2}}{1 + h_{fe2}} \right) \]

Model Graph (Frequency Response) :-

\[ \text{gain (dB)} \]

\[ |A_v| \]

\[ f_{L1}, f_{L2}, f_{h1}, f_{h2} \quad \text{Frequency (Hz)} \]
**General Procedure for Calculation:**

1. **Input impedance**
   a. Connect a Decade Resistance Box (DRB) between input voltage source and the base of the transistor (series connection).
   b. Connect ac voltmeter (0-100mV) across the biasing resistor $R_2$.
   c. Vary the value of DRB such that the ac voltmeter reads the voltage half of the input signal.
   d. Note down the resistance of the DRB, which is the input impedance.

2. **Output impedance**
   a. Measure the output voltage when the amplifier is operating in the mid-band frequency with load resistance connected ($V_{load}$).
   b. Measure the output voltage when the amplifier is operating in the mid-band frequency without load resistance connected ($V_{no-load}$).
   c. Substitute these values in the formula

   \[ Z_o = \frac{V_{load} - V_{no-load}}{V_{load}} \times 100\% \]

3. **Bandwidth**
   a. Plot the frequency response
   b. Identify the maximum gain region.
   c. Drop a horizontal line bi –3dB.
   d. The –3dB line intersects the frequency response plot at two points.
   e. The lower intersecting point of –3dB line with the frequency response plot gives the lower cut-off frequency.
   f. The upper intersecting point of –3dB line with the frequency response plot gives the upper cut-off frequency.
   g. The difference between upper cut-off frequency and lower cut-off frequency is called Bandwidth. Thus Bandwidth = $f_h - f_l$. 

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### With Feedback \((V_i = 50\text{mV})\)

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### Without Feedback \((V_i = 50\text{mV})\)

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Circuit Diagram:

Design
Given $f_0 = 1 \text{ kHz}; C = 0.01 \mu \text{F}, V_{CC} = 12 \text{ V}$

$$f = \frac{1}{2\pi \sqrt{6RC}}$$

Find R

$$\beta(s) = -\frac{1}{29}$$

$$A = \frac{1}{\beta} = -29$$

Amplifier Design

Gain formula is given by,

$$A_v = -\frac{h_{fe} R_{\text{Eff}}}{h_{ie}}$$  \hspace{1cm} (A_v = 29, design given)

Assume $V_{CE} = V_{CC}/2$ (transistor Active)

Effective load resistance is given by, $R_{\text{Eff}} = R_C || R_L$

Emitter resistance is given by, $R_E = 26 \text{ mV} / I_E$

$$h_{ie} = \beta r_e$$

Where $r_e$ is internal resistance of the transistor.

$$h_{ie} = h_{fe} r_e$$

$$V_E = V_{CC} / 10$$
Experiment No: DATE: __/__/____

**RC PHASE SHIFT OSCILLATOR**

**AIM:** To design and test for the performance of RC Phase Shift Oscillator for the given operating frequency $f_o$.

**APPARATUS REQUIRED:**
- Transistor - BC 107, capacitors, resistor, power supply, CRO, multimeter, etc.

**PROCEDURE:**
1. Connect the circuit as per the circuit diagram (both oscillators).
2. Switch on the power supply and observe the output on the CRO (sine wave).
3. Note down the practical frequency and compare with its theoretical frequency.
on applying KVL to output loop, we get:

\[ V_{CC} = I_C R_C + V_{CE} + I_E R_E \]

where \( V_E = I_E R_E \)

Find \( R_C \).

Since \( I_B \) is very small when compared with \( I_C \),

\[ I_C \approx I_E \]

\[ R_E = \frac{V_E}{I_E} \]

\[ V_B = V_{BE} + V_E \]

\[ V_B = V_{CC} \frac{R_{R2}}{R_{R1} + R_{R2}} \]

\[ S = 1 + \frac{R_B}{R_E} \]

Find \( R_B \).

\[ R_B = R_{R1} \parallel R_{R2} \]

Find \( R_{R1} \) and \( R_{R2} \).

Coupling and bypass capacitors can be found out by,

Input coupling capacitor is given by, \( X_{C1} = \{[h_{ie} + (1 + h_{fe}) R_E] \parallel R_B\} / 10 \)

\[ X_{C1} = \frac{1}{2 \pi f C_i} \]

Find \( C_i \).

\[ X_{C0} = \frac{1}{2 \pi f C_0} \]

Find \( C_0 \).

By-pass capacitor is given by, \( X_{CE} = R_E / 10 \)

\[ X_E = \frac{1}{2 \pi f C_E} \]

Find \( C_E \).
## Result

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HARTLEY OSCILLATOR:-

**DESIGN:-**

\[ f = \frac{1}{2\pi \sqrt{LC}}, \text{ where } L = L1 + L2 \]

Assume \( \frac{L2}{L1} = 5 \), Let \( L1 = 2 \text{mH} \). \( \therefore L2 = 10 \text{mH} \)

Let \( Vgs = -1.5 \text{V} \). \( \therefore Id = Idss \left(1 - \frac{Vgs}{Vp}\right) = 3 \text{mA} \)

\[ g_m = \frac{-2Idss}{Vp} \left(1 - \frac{Vgs}{Vp}\right) = 4 \text{mhos} \]

\[ R_S = \frac{V_s}{Id} = \frac{-Vgs}{Id} = \frac{1.5}{3m} = 500 \Omega \]

Assume \( Av = 10 \) \( \left( > \frac{L2}{L1} \right) \Rightarrow 10 = g_m R_d \)

\[ \therefore R_d = \frac{10}{4m} = 2.5 \text{K}\Omega \]

Assume \( R_g = 1 \text{M}\Omega \), \( Cc1 = Cc2 = 0.1 \mu \text{f} \), \( Cs = 47 \mu \text{f} \)

Assuming \( Vds = 5 \text{V} \)

\[ \therefore Vdd = IdRd + Vds + Vs = 14 \text{V} \]
Experiment No: __/__/____

HARTLEY AND COLPITTS OSCILLATOR

AIM:

To design and test for the performance of FET – Hartley & Colpitt’s Oscillators.

APPARATUS REQUIRED:

Transistor – BFW10, capacitors, resistor, power supply, CRO, function generator, multimeter, etc.

PROCEDURE:

1. Connect the circuit as per the circuit diagram (both oscillators).
2. Switch on the power supply and observe the output on the CRO (sine wave).
3. Note down the practical frequency and compare with its theoretical frequency.
**COLPITTS OSCILLATOR:**

**DESIGN:**

\[ f = \frac{1}{2\pi \sqrt{LC}} \text{, where } \frac{C_1C_2}{C_1 + C_2} \]

Assume \( \frac{C_1}{C_2} = 5 \), Let C1=500pF : C2=100pF

\( \therefore L = 0.12 \text{H, for } f=50 \text{KHz} \)

Let Vgs = -1.5V, \( \therefore I_d = I_d = I_{dss} - \left( \frac{V_{gs2}}{V_p} \right) = 3 \text{mA} \)

\[ g_m = -\frac{2I_{dss}}{V_p} = -\frac{V_{gs}}{V_p} = 4 \text{mhos} \]

\[ \therefore R_s = \frac{V_s}{I_d} = -\frac{V_{gs}}{I_d} = 1.5 \therefore 3m = 500\Omega \]

Assume \( A_v = 10 \) (\( > \frac{C_1}{C_2} \)) \( \Rightarrow 10 = g_m R_d \)

\[ \therefore R_d = \frac{10}{4m} = 2.5K\Omega \]

Assume \( R_g = 1M\Omega \), Cc1=Cc2=0.1µF, Cs=47 µF, assuming Vds=5V

\[ \therefore V_{dd} = I_d R_d + V_{ds} + V_s = 14V \]
**DESIGN:**

\[ f = \frac{1}{2\pi\sqrt{LC}} \]

Assume \( L = 0.33 \text{H} \), \( C = 0.0767 \text{pF} \)

Let \( V_{ce} = 6 \text{V} \), \( I_c = 2 \text{mA} \)

Choose \( V_{cc} = 2 V_{ce} \)

Assume \( V_e = \frac{V_{cc}}{10} = 1.2 \text{V} \)

\[ R_e = \frac{V_e}{I_e} = \frac{V_e}{I_c} = 1.2 \text{V} \]

\[ R_e = \frac{V_e}{I_e} = \frac{V_e}{I_c} = 1.2 \frac{2}{2m} = 600 \Omega \]

\[ R_1 = 34K\Omega \]

\[ R_c = \frac{V_{cc} - V_{ce} - V_{re}}{I_{cl}} = \frac{12 - 6 - 1.2}{2m} = 2.4K\Omega \]

Assume \( C_{c1} = C_{c2} = 0.1 \mu\text{f} \), \( C_e = 47 \mu\text{f} \)

**Result:**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Theoretical</th>
<th>Practical</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>Hartley</td>
<td>Colpitt</td>
</tr>
<tr>
<td></td>
<td>Hartley</td>
<td>Colpitt</td>
</tr>
</tbody>
</table>
Circuit Diagram:-

Series Clippers

a) To pass –ve peak above Vr level :-

b) To pass –ve peak above some level (say –3v) :-
AIM:
To design a Clipping circuit for the given specifications and hence to plot its O/P

APPARATUS REQUIRED:-
Diode-IN 4007, capacitors, resistor, power supply, CRO, function generator, multimeter, etc.

PROCEDURE: -
1. Connections are made as shown in the circuit diagram.
2. A sine wave Input Vi whose amplitude is greater than the clipping level is applied.
3. Output waveform Vo is observed on the CRO.
4. Clipped voltage is measured and verified with the designed values.
c) To pass +ve peak above Vr level :-

\[ \text{Diagram of circuit with +ve peak above Vr level.} \]

\[ \text{Diagram showing voltage vs. time.} \]

\[ \text{Diagram of voltage vs. voltage.} \]

\[ \text{Diagram showing voltage vs. voltage.} \]

\[ \text{Diagram showing voltage vs. voltage.} \]

d) To pass +ve peak above some level (say +3v) :-

\[ \text{Diagram of circuit with +ve peak above +3v level.} \]

\[ \text{Diagram showing voltage vs. time.} \]

\[ \text{Diagram of voltage vs. voltage.} \]

\[ \text{Diagram showing voltage vs. voltage.} \]

\[ \text{Diagram showing voltage vs. voltage.} \]
Design :-

Choose $R_f = 10\Omega$, $R_r = 1M\Omega$

\[ R = \sqrt{R_f R_r} = 3.3K\Omega \]

a) To pass $-ve$ peak above $V_r$ level

b) To pass $-ve$ peak above some level (say $-3v$)
   
   \[ - (V_r + V_r) = -3 \]
   \[ V_r = 3 - V_r \]
   \[ 3 - 0.6 = 2.4v \]

c) To pass $+ve$ peak above $V_r$ level

d) To pass $+ve$ peak above some level (say $+3v$)
   
   \[ (V_r + V_r) = +3 \]
   \[ V_r = 3 - 0.6 = 2.4v \]

e) To pass $+ve$ peak above some level (say $+4v$) and $-ve$ peak above some level (say $-3v$)
   
   \[ V_r + V_r = 4 \]
   \[ V_r = 3.4v \]
   \[ - (V_r + V_r) = -3v \]
   \[ V_r = 2.4v \]

f) To remove $+ve$ peak above $V_r$ level

g) To remove $+ve$ peak above some level (say $3v$)
   
   \[ (V_r + V_r) = 3v \]
   \[ V_r = 2.4v \]

h) To pass $-ve$ peak above some level (say $-2v$)
   
   \[ -V_r + V_r = -2 \]
   \[ V_r = 2.6v \]
e) To pass +ve peak above some level (say +4v) & -ve peak above some level (say -3v) :-

Shunt Clippers

f) To remove +ve peak above Vr level :-
i) To remove –ve peak above Vr level

j) To pass +ve peak above some level (say 2v)
   ie., VR-Vr = 2
   VR = 2.6v

k) To remove –ve peak above some level (say -3v)
   ie., -(VR+Vr) = -3
   VR = 2.4v

l) To remove +ve peak above some level (say +3v) and –ve peak above some level (say -3v)
   ie., (VR1+Vr) = 3v
   VR1 = 2.4v
   -(VR2+Vr) = -3v
   VR2 = 2.4v

m) To pass a part of the +ve half cycle (say V1 = 2v, V2 = 4.2v)
   ie., (VR1 - Vr) = 2v
   VR1 = 2.6v
   (VR2+Vr) = 4.2v
   VR2 = 3.6v
g) To remove +ve peak above some level (say +3V) :-

![Circuit Diagram](image1)

- Diagram showing the circuit for removing +ve peaks above +3V.

h) To pass –ve peak above some level (say -2V) :-

![Circuit Diagram](image2)

- Diagram showing the circuit for passing –ve peaks above -2V.
i) To remove above \( V_r \) level :-

\[ \text{Diagram of circuit to remove above } V_r \text{ level} \]

\[ \text{Graph of output voltage } V_o \text{ against input voltage } V_i \]

j) To pass +ve peak above some level (say +2v) :-

\[ \text{Diagram of circuit to pass +ve peak above +2v} \]

\[ \text{Graph of output voltage } V_o \text{ against input voltage } V_i \]
k) To remove $-ve$ peak above some level (say $-3v$):

![Circuit Diagram]

l) To remove above some level (say $+3v$) and $-ve$ peak above some level (say $-3v$):

![Circuit Diagram]
m) To pass a part of the positive half cycle (say V1 = 2v, V2 = 4.2v):
Circuit Diagram:

a) Positive peak clamped at Vr level:

b) Positive peak clamped at +ve Reference:
AIM: To design a Clamping circuit for the given specifications and hence to plot its output.

APPARATUS REQUIRED: Diode-IN 4007, capacitors, resistors, power supply, CRO, function generator, multimeter, etc.

PROCEDURE:
1. Connections are made as shown in the circuit diagram.
2. A square wave input $V_i$ is applied
3. Output waveform $V_o$ is observed on the CRO. Keeping the AC/DC switch of the CRO in DC Position.
4. Clamped voltage is measured and verified with the designed values.
c) Positive peak clamped at –ve reference level :-

d) Negative peak clamped to Vr level :-
DESIGN :-

\[ RLC >> T \Rightarrow \text{Assume } T = 2 \text{ ms, let } RLC = 50T = 100\text{ms} \]

Let \( R_L = 100\text{K}\Omega \)

\[ \therefore C = 1\mu\text{f} \]

a) Positive peak clamped to \( V_r \) level

b) Positive clamped to +ve reference level (say +2v)

\[ \text{ie., } VR + V_r = 2 \Rightarrow VR = 2 - V_r = 2 - 0.6 = 1.4\text{v} \]

c) Positive peak clamped to –ve reference level (say -2v)

\[ \text{ie., } -VR + V_r = -2 \Rightarrow VR = 2.6\text{v} \]

d) Negative peak clamped to \( V_r \) level

e) Negative peak clamped to +ve reference level (say +2v)

\[ \text{ie., } VR - V_r = 2 \Rightarrow VR = 2.6\text{v} \]

f) Negative peak clamped to –ve reference level (say -2v)

\[ \text{ie., } (VR + V_r) = -2 \Rightarrow VR = 1.6\text{v} \]
e) Negative peak clamped at +ve reference level :-

f) Negative peak clamped at –ve reference level :-
**RESULT :-**

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Clamping level (Designed)</th>
<th>Clamping level (Observed)</th>
</tr>
</thead>
<tbody>
<tr>
<td>a)</td>
<td></td>
<td></td>
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<tr>
<td>b)</td>
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<tr>
<td>c)</td>
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<td>d)</td>
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<tr>
<td>e)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>f)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Circuit Diagram:-

INVERTING AMPLIFIER:-

NONINVERTING AMPLIFIER:-

VOLTAGE FOLLOWER:-
LINEAR APPLICATIONS OF OP-AMP

AIM: To design and test Operational amplifier applications: (1)Inverting Amplifier, (2) Non-Inverting Amplifier, (3) Summer, (4) Voltage Follower, (5) Integrator and Differentiator.

APPARATUS REQUIRED: Op-Amp – μA 741, capacitors, resistor, Dual power supply, Regulated power supply, CRO, function generator, multimeter, etc.

PROCEDURE: -
1. Connect the circuit as per the circuit diagram.
2. Give the input signal as specified.
3. Switch on the dual power supply.
4. Note down the outputs from the CRO.
5. Draw the necessary waveforms on the graph sheet.
6. Repeat the procedure for all circuits.

DESIGN:-

a) Inverting Amplifier: Let $Av = 10 = \frac{-R_f}{R_i}$
Assume $R_i = 1\,\text{k}\Omega$ ∴ $R_f = 10\,\text{K}\Omega, R_i = 10\,\text{K}\Omega$

b) Non Inverting Amplifier Let $Av = 11 = 1 + \frac{R_f}{R_i}$
Assume $R_i = 1\,\text{k}\Omega$ ∴ $R_f = (11-1) \times R_i = 10\,\text{k}\Omega$

c) Voltage follower $Av =$unity.
**SUMMER:**

![Summer Circuit Diagram](image)

**DIFFERENTIATOR:**

![Differentiator Circuit Diagram](image)

**INTEGRATOR:**

![Integrator Circuit Diagram](image)
**DESIGN:**

**a) Integrator**

RC >> T

Let T = 1 msec and RC = 100 T = 100 msec

Assume R = 100 KΩ :. C = 1 μF

Assume Rf = 10 KΩ

**b) Differentiator:**

RC << T

Let T = 1 msec and Rc = 0.01 μF

Assume R = 1 KΩ

**c) Summer:**

Let Y = 2V1 + V2 + 3V3 = \( \frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \)

i.e., :. \( \frac{R_f}{R_1} = 2, \frac{R_f}{R_2} = 1 \) and \( \frac{R_f}{R_3} V_3 \)

Assume Fr = 10 kΩ :. R1 = 5 KΩ, R2 = 10 kΩ and R3 = 3.33 kΩ

Assume R = 10 kΩ
Circuit Diagram:-

Schmitt trigger with zero-reference

\[
V_i = 1V \\
\text{freq} = 1 \text{kHz}
\]

\[V_o = A(V_b - V_i)\]

Schmitt trigger with positive reference

Comparator: Zero Crossing Detector

\[V_0 = +V_{sat}, \text{ when } V_i < 0\]
\[V_0 = -V_{sat}, \text{ when } V_i > 0\]
Experiment No: ___________________ DATE: __/__/____

SCHMITT TRIGGER

To design and test USING Operational amplifiers for the performance of:

AIM: 
(1) Zero Crossing Detector, (2) Schmitt Trigger for different hysteresis values.

APPARATUS REQUIRED:-
Op-Amp – μA 741, capacitors, resistor, Dual power supply, Regulated power supply, CRO, function generator, multimeter, etc.

PROCEDURE: -
1. Connect the circuit as per the circuit diagram.
2. For a zero crossing detector, connect the non-inverting terminal to ground.
3. Switch on the dual power supply.
4. Observe the output waveform on the CRO.
5. Draw the output and input waveforms.
6. For Schmitt Trigger set input signal (say 1V, 1 KHz) using signal generator.
7. Observe the input and output waveforms on the CRO.
8. Plot the graphs: V_i vs Time, V_o vs Time.
Schmitt trigger with negative reference

Design
Given, \( V_R = 0 \) and \( \pm V_{\text{sat}} = \pm 12 \, \text{V} \).
Assume, \( V_{h1} = V_{h2} \)

WAVE FORMS:-
DESIGN:-

Let UTP = 6V = \( \frac{VRRI}{R1 + R2} + \frac{V_{sat}R2}{R1 + R2} \)

LTP = - 2V = \( \frac{VRRI}{R1 + R2} + \frac{V_{sat}R2}{R1 + R2} \)

Assume \( V_{sat} = 12V \)

\[
\begin{align*}
\text{UTP} + \text{LTP} = 4 & = \frac{2VRRI}{R1 + R2} \Rightarrow VR = \frac{2(R1 + R2)}{R1} = 2(1 + \frac{R2}{R1}) \\
\text{UTP} - \text{LTP} = 8 & = \frac{2V_{sat}R2}{R1 + R2} \Rightarrow VR = \frac{R1}{R2} = 2
\end{align*}
\]

\( \therefore \) \( VR = 3V \), Assume \( R2 = 1 \, \text{K\Omega} \) \( \Rightarrow R1 = 2 \, \text{K\Omega} \)

III\textsuperscript{y} design for UTP = +4, +8, +2 and -2.

LTP = - 4, + 2, - 4 and = 4

RESULT: -UTP and LTP is measured and compared with the designed value.
FULL WAVE PRECISION RECTIFIER:

![Diagram of a full wave precision rectifier]

**DESIGN:**

(i) Given $A = \frac{5}{0.5} = 10 = \frac{R_f}{R_i}$

Assume $R_i = 1\, \text{k}\Omega$, $\therefore R_f = 10\, \text{k}\Omega$

Choose $R = 10\, \text{k}\Omega$

$R_f' = R_f = 10\, \text{k}\Omega$

(ii) Given $A1 = \frac{5}{0.5} = 10 = \frac{R_f}{R_i}$ and $A2 = \frac{3}{0.5} = 6 = 3 \frac{R_f}{R_i} \left( \frac{R_f'}{2R + R_f'} \right)$

Assume $R_i = 1\, \text{k}\Omega$

$R_f = 10\, \text{k}\Omega$ and $R_f' = 5\, \text{k}\Omega$
Experiment No:          DATE: __/__/____

FULL WAVE PRECISION RECTIFIER

AIM:  To test for the performance of Full wave Precision Rectifier using Operational Amplifier.

APPARATUS REQUIRED:-
Op-Amp – µA 741, capacitors, resistor, Dual power supply, Regulated power supply, CRO, function generator, multimeter, etc.

PROCEDURE: -
1. Connect the circuit as per the circuit diagram.
2. Give a sinusoidal input of VPP, 1 KHz from a signal generator.
3. Switch on the power supply and note down the output from CRO.
4. Without Connecting Rf 2, the wave form of the half wave rectifier is produced.
5. At some value of Rf 2 the wave form of a full wave rectifier is obtained.
6. Repeat the above procedure by reversing the diodes.

RESULT:-
The operation of the precision rectifier is studied using µA 741.
CIRCUIT DIAGRAM: - (HIGH VOLTAGE)

DESIGN:-

Given $V_o = 12v$

$$V_o = 7.15 \left[ 1 + \frac{R_1}{R_2} \right]$$

$$12 = 7.15 \left[ 1 + \frac{R_1}{R_2} \right]$$

Assume $R_1 = 10K\Omega$

$\therefore R_2 = 17.7K\Omega$ [use 15K\Omega]

Assume $R_L = 720\Omega$ & $C = 100pf$

CHARACTERISTIC CURVE: -

![Characteristics Curve Graph]

<table>
<thead>
<tr>
<th>Vi (volts)</th>
<th>Vo (volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>7v</td>
<td></td>
</tr>
</tbody>
</table>
Experiment No:  

DATE: __/__/____

**VOLTAGE REGULATOR USING IC 723**

**AIM:** To design and test the IC 723 voltage regulator.

**APPARATUS REQUIRED:**
- IC 723, capacitors, resistor, power supply, CRO, function generator, multimeter, etc.

**PROCEDURE:**
1. Connect the circuit as per the circuit diagram.
2. Switch on the power supply and note down the output from CRO.
3. Vary the input voltage from 7V, note down corresponding output voltage.
4. Draw the regulation characteristics.
CIRCUIT DIAGRAM: - (LOW VOLTAGE)

DESIGN:-

For LM723 \( V_{ref} = 7.15\text{V} \)

\[
V_o = 7.15 \left[ \frac{R_2}{R_1 + 2} \right]
\]

Let the divider current \( I_o \) through the resistor \( R_1 \) & \( R_2 \) is 1mA. Since error amplifier draws very little current, we will neglect its input bias current.

Hence \( R_1 = \frac{V_{ref} - V_o}{I_o} = \frac{7.15 - 6}{1 \times 10^{-3}} = 1.1\text{K} \Omega \)

\( R_2 = \frac{V_o}{I_o} = \frac{6}{1 \times 10^{-3}} = 6\text{K} \Omega \)

\( R_3 = \frac{R_1 R_2}{R_1 + R_2} \)

Assume \( C_1 = 0.1\mu\text{F} \) & \( C_2 = 100\text{PF} \)
PROCEDURE:

1. Connect the circuit as per the circuit diagram.

2. For line regulation vary the input voltage from 7V, note down the corresponding output voltage.

3. Draw the transfer characteristics.

4. For load regulation note down the output current.

5. Draw the transfer characteristics.

GRAPH:

(i) Line Regulation  
(ii) Load Regulation

OBSERVATION:

<table>
<thead>
<tr>
<th>(i) Line Regulation</th>
<th>(ii) Load Regulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vi (volts)</td>
<td>Vo (volts)</td>
</tr>
<tr>
<td>Vi (volts)</td>
<td>Vo (volts)</td>
</tr>
<tr>
<td>Io (mA)</td>
<td>Vo (volts)</td>
</tr>
</tbody>
</table>
CIRCUIT DIAGRAM: -

\[ V_o = -R_f \left[ \frac{b_3}{2R} + \frac{b_2}{4R} + \frac{b_1}{8R} + \frac{b_0}{16R} \right] \times V_{ref} \]

Note: -
1. \(b_3, b_2, b_1\) and \(b_0\) are binary input.
2. \(V_{ref} = 5V\).
3. If \(b\) is the decimal value of the binary input \(b_3, b_2, b_1, b_0\), then \(V_o = -\frac{V_{ref}}{8} \times b\)
4. \(V_o\) is the analog output
5. Binary inputs can either take the value 0 or 1
6. Binary input \(b_i\) can be made 0 by connecting the input to the ground. It can be made 1 by connecting to +5V
VOLTAGE REGULATOR USING IC 723

AIM: - To design 4 bit R-2R ladder DAC using op-amp.

APPARATUS REQUIRED:-
IC 723, resistor, power supply, CRO, multimeter, etc.

PROCEDURE: -
1. Connect the circuit as per the circuit diagram.
2. The IC is given proper bias of ‘+12V’ and ‘-12V’ to ‘Vcc’ and ‘Vee’ respectively.
3. According to the binary values of b₃, b₂, b₁ and b₀, b₃, b₂, b₁ and b₀ are connected to ‘+5V’ or ‘Ground’ respectively.
4. The o/p voltage is tabulated for different binary inputs and is compared with the theoretical values.
O/P vs I/P

Decimal equivalent of binary input (b3, b2, b1, b0)

-0.625V
-1.25V
-1.875V
-9.375V

O/P voltages
in volts

0 1 2 3 4 5 6 //
14 15
Tabular Column:

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output (volts)</th>
<th>Practical</th>
<th>Theoretical</th>
</tr>
</thead>
<tbody>
<tr>
<td>b₃ b₂ b₁ b₀</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 0 0 0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 0 0 1</td>
<td></td>
<td></td>
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<tr>
<td>0 0 1 0</td>
<td></td>
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<td>0 0 1 1</td>
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<td>0 1 0 0</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>0 1 0 1</td>
<td></td>
<td></td>
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<td>0 1 1 0</td>
<td></td>
<td></td>
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<td>0 1 1 1</td>
<td></td>
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<tr>
<td>1 0 0 0</td>
<td></td>
<td></td>
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<td>1 0 0 1</td>
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<td>1 0 1 0</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>1 0 1 1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 1 0 0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 1 0 1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 1 1 0</td>
<td></td>
<td></td>
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<tr>
<td>1 1 1 1</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
CIRCUIT DIAGRAM: - (2 BIT Flash type ADC)
AIM: To rig up circuit to convert an analog voltage to its digital equivalent

APPARATUS REQUIRED:

IC LM 324, IC 7400, resistor, power supply, multimeter, etc.

PROCEDURE:

1. Connect the circuit as per the circuit diagram.
2. Verify the digital O/P for different analog voltages.

Note: (1). Connect V+ (pin 4) terminal of the OPAMP to +5V
       (2). Connect V- (pin 11) terminal of the OPAMP to ground

Design: Number of comparators required = 2n-1

Where n = desired number of bits
C1, C2 & C3 = Comparator o/p
D0 & D1 = Encoder (Coding network) O/P
PIN DIAGRAM:-

![PIN Diagram of LM324](image-url)
<table>
<thead>
<tr>
<th>Analog I/P Vin</th>
<th>C3</th>
<th>C2</th>
<th>C1</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 to v/4</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>V/4 to V/2</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>V/2 to 3V/4</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>3V/4 to V</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>